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(19) **United States**(12) **Patent Application Publication**
Sakamoto et al.(10) **Pub. No.: US 2006/0279202 A1**(43) **Pub. Date: Dec. 14, 2006**(54) **VAPOR DEPOSITION MASK, ORGANIC
ELECTROLUMINESCENT DISPLAY
DEVICE, AND MANUFACTURING METHOD
THEREFOR****Publication Classification**(51) **Int. Cl.****H05B 33/00** (2006.01)**H01L 51/50** (2006.01)**B05D 5/06** (2006.01)**B05D 5/12** (2006.01)**B05C 11/11** (2006.01)(52) **U.S. Cl.** **313/504; 313/503; 427/66;
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Minami-Ashigara-shi (JP)(57) **ABSTRACT**(21) Appl. No.: **11/441,204**(22) Filed: **May 26, 2006**(30) **Foreign Application Priority Data**

May 27, 2005 (JP) 2005-155615

In an organic electroluminescent display device comprising a wiring layer, an insulating layer, a first electrode, an organic electroluminescent layer, and a second electrode, wiring which conducts with a second electrode is arranged between light emitting pixels, and is provided either between an organic electroluminescent layer and the second electrodes, or on top of the second electrodes.

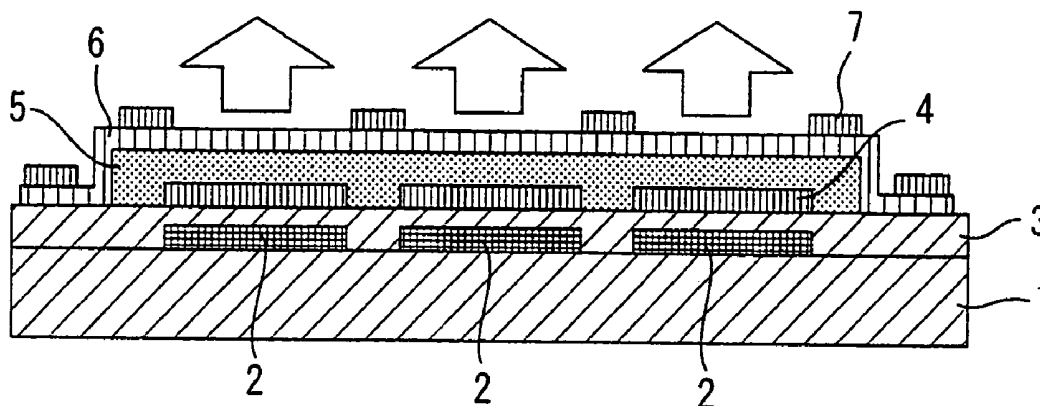


FIG. 1

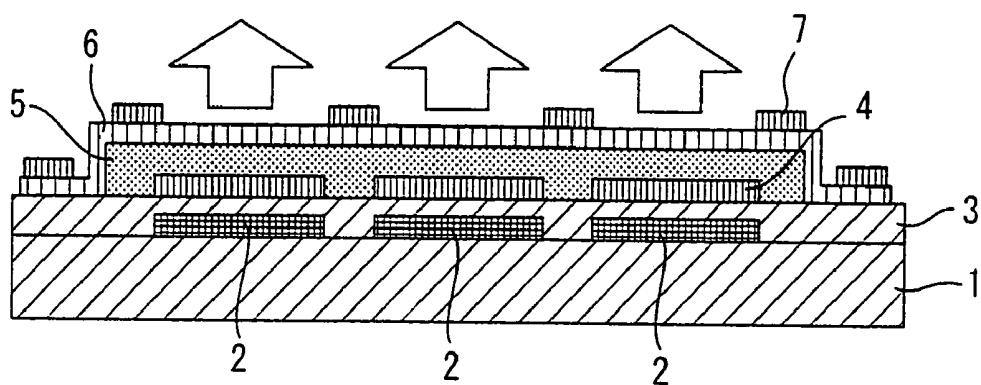


FIG. 2

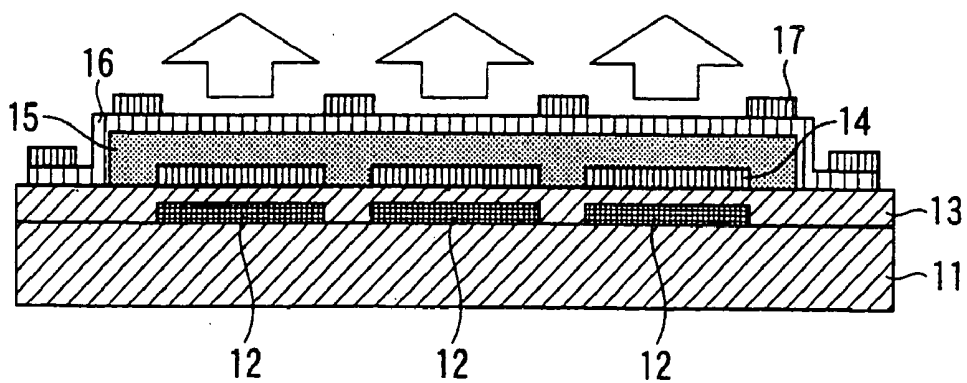


FIG. 3

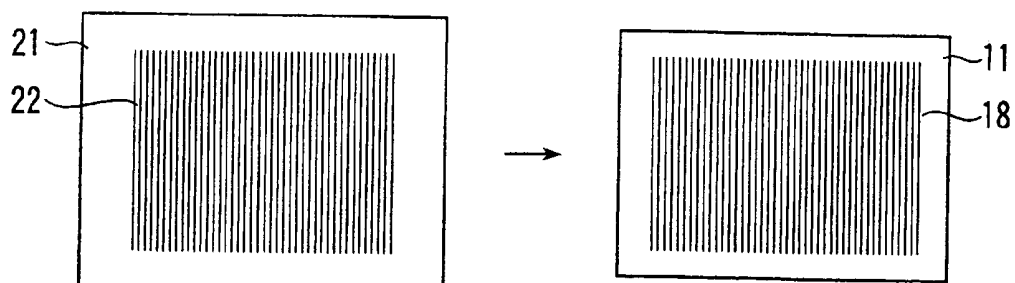


FIG. 4

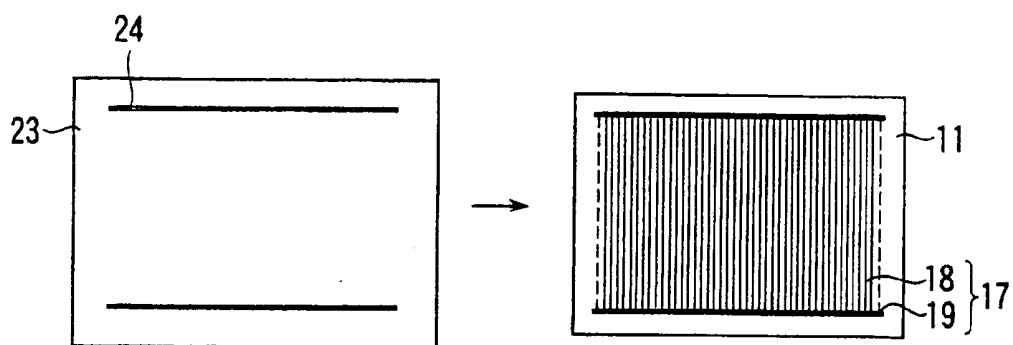


FIG. 5A

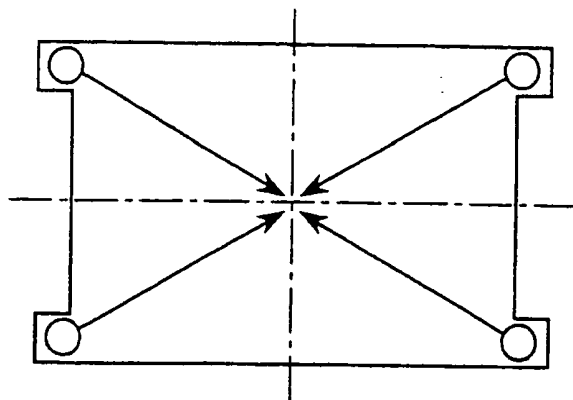


FIG. 5B

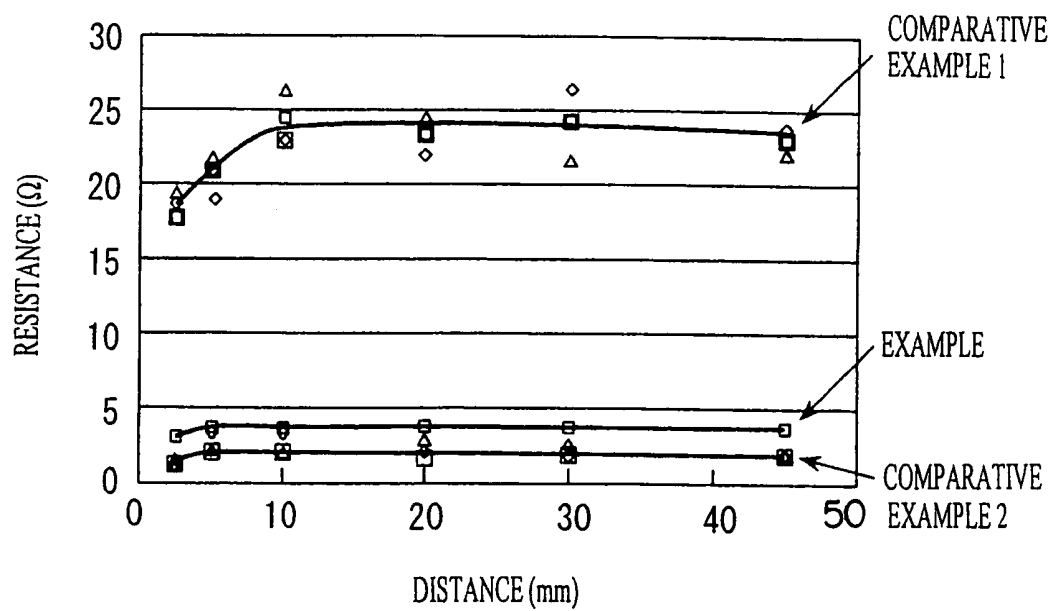


FIG. 6

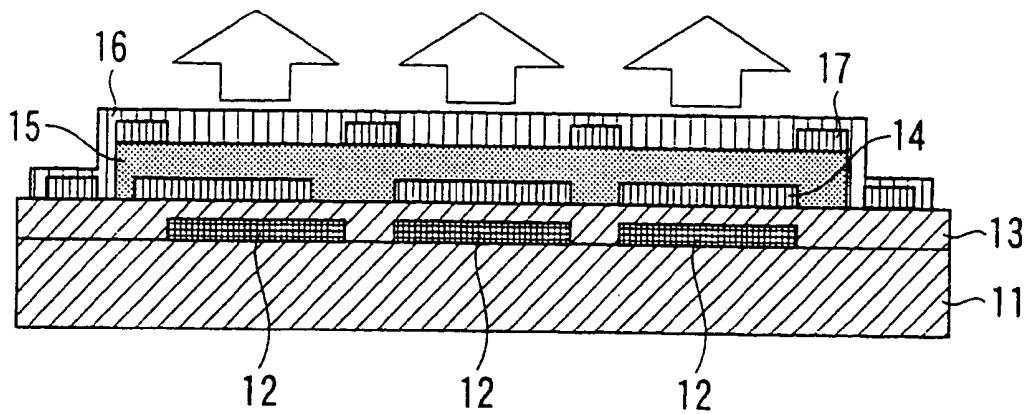


FIG. 7

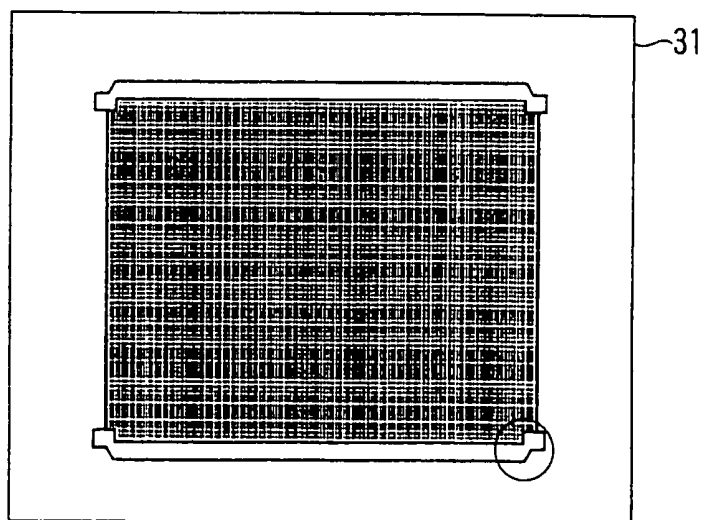


FIG. 8

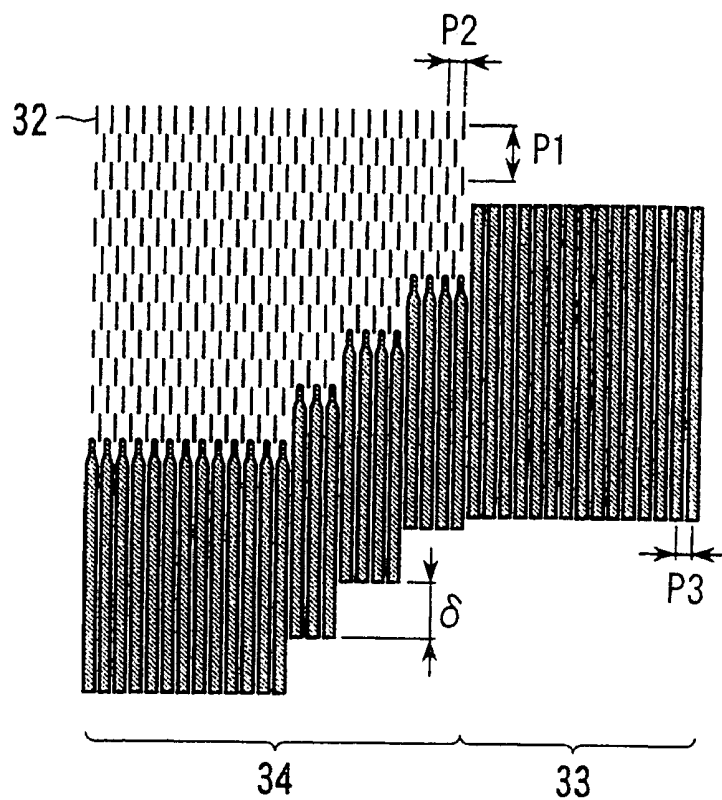
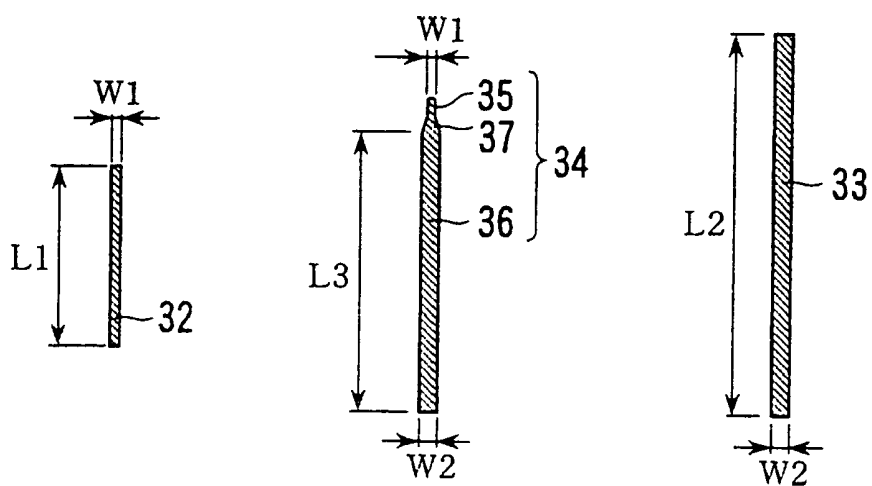


FIG. 9



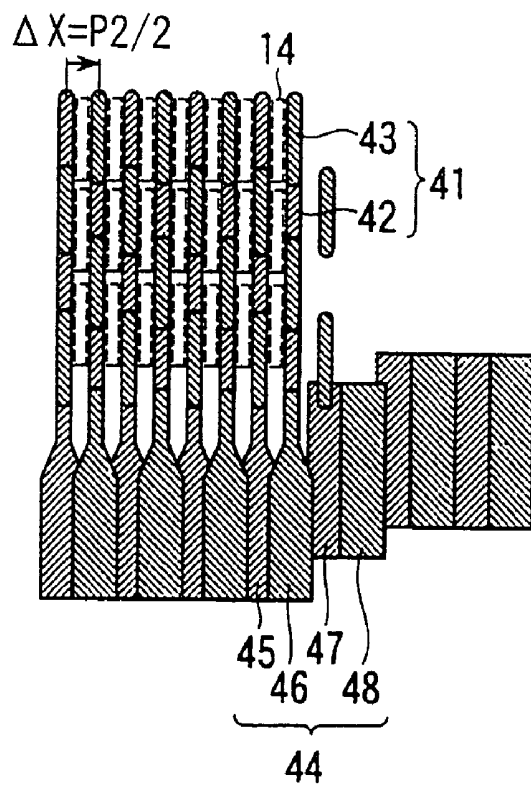
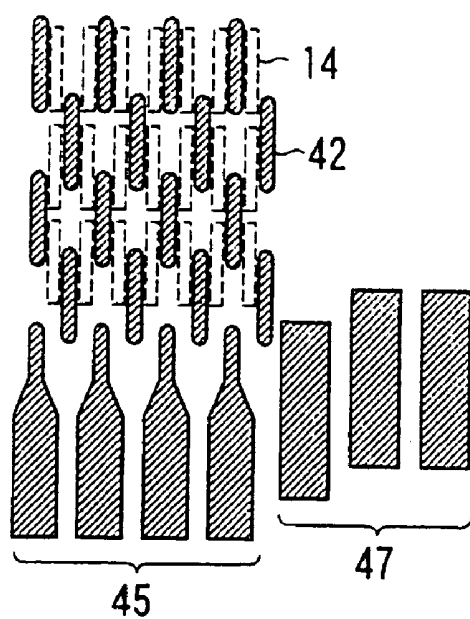


FIG. 10

FIG. 11

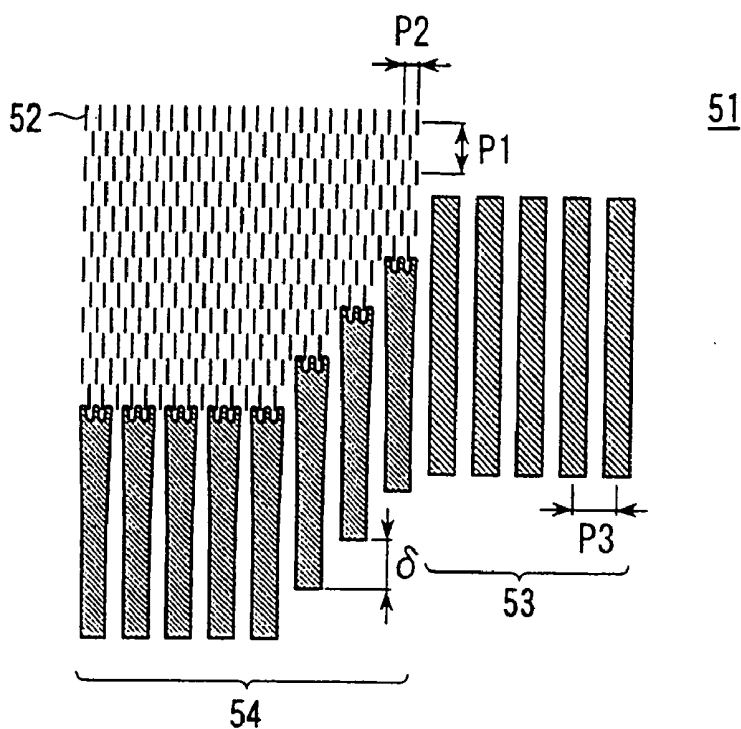
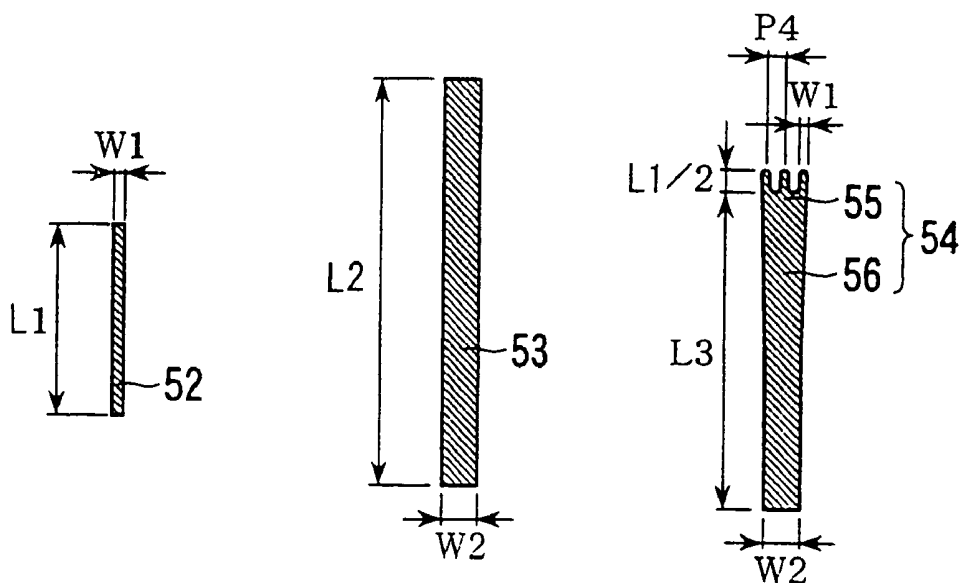
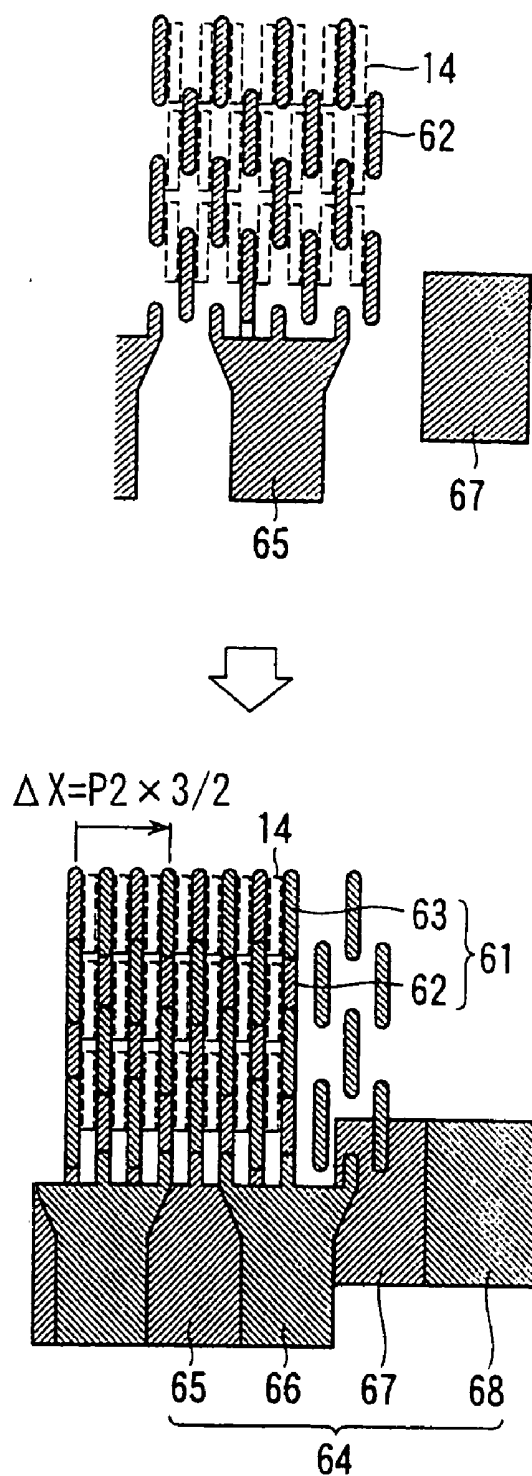
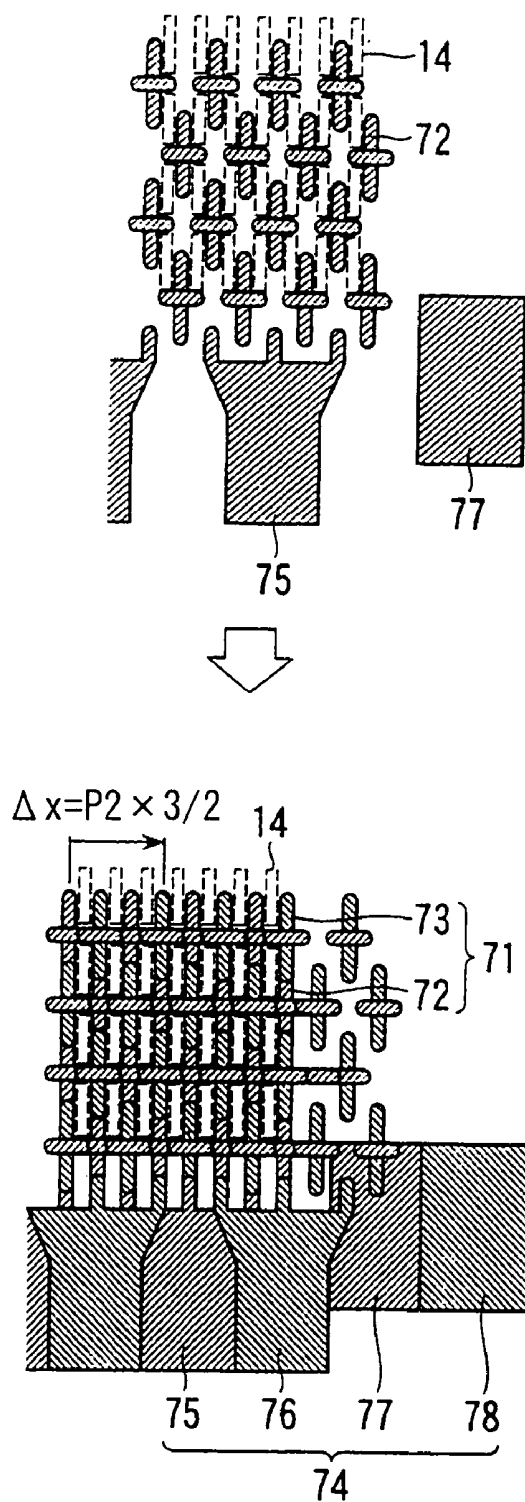
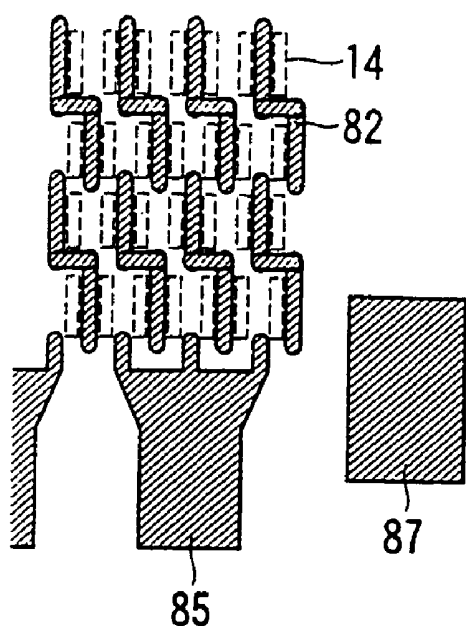


FIG. 12









$$\Delta X = P2 \times 3/2$$

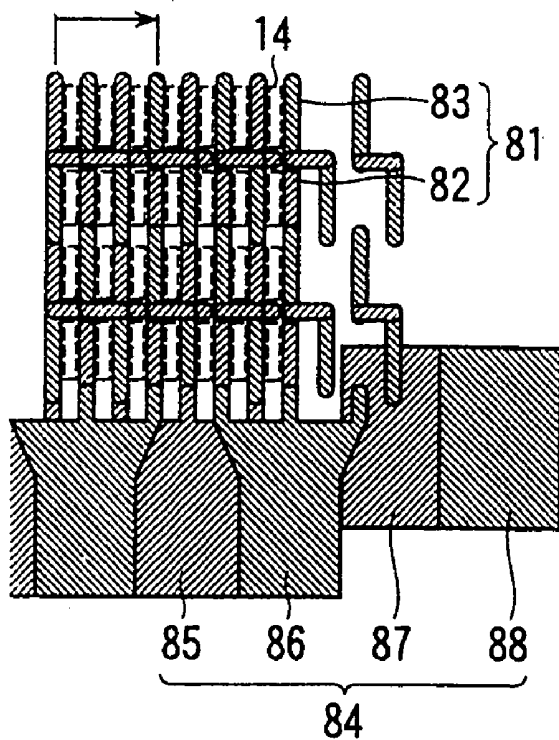
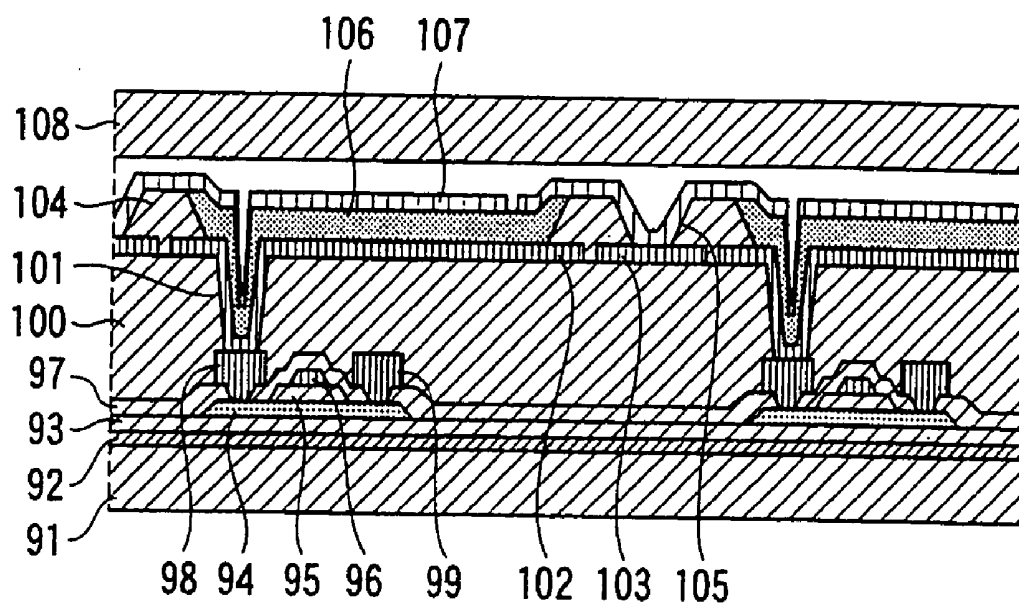


FIG. 15

FIG. 16



VAPOR DEPOSITION MASK, ORGANIC ELECTROLUMINESCENT DISPLAY DEVICE, AND MANUFACTURING METHOD THEREFOR

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 USC 119 from Japanese Patent Application, No.2005-155615, the disclosure of which is incorporated by reference herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a vapor deposition mask, an organic electroluminescent (hereunder EL) display device, and a manufacturing method therefor. In particular the present invention relates to a vapor deposition mask in an active matrix drive organic EL display device of a top emission type, an organic EL display device, and a manufacturing method therefor.

[0004] 2. Description of the Related Art

[0005] As a display device which can be made thin and lightweight as compared to conventional cathode-ray tubes (CRT) and liquid crystal displays (LCD), a display device using organic EL elements has recently attracted a great deal of attention.

[0006] Since the organic EL element is self light emitting, it has various characteristics such as, the visibility is high, there is no viewing angle dependency, a film substrate having flexibility can be used, and it is thin and lightweight as compared to the liquid crystal display.

[0007] In conventional organic EL display devices, for example an anode made from a transparent conductive film such as indium tin oxide film (hereunder ITO) is formed on an insulation substrate made from a glass substrate, and on this anode is formed an organic EL layer containing a luminous layer which generates light by recombination of electrons and positive holes. Furthermore, on the organic EL layer is formed a cathode made from Al or Mg—Ag alloy or the like. That is to say, on the insulation substrate is formed the anode, the organic EL layer, and an organic EL element comprising the cathode. Normally, the light generated in the luminous layer of the organic EL layer is emitted from the insulation substrate side, giving a so-called bottom emission type.

[0008] Furthermore, in order to realize a high definition display, advance is being made together with the organic EL element, for the development of a display device of an active matrix type having switching elements such as thin film transistors (hereunder TFT).

[0009] In the aforementioned bottom emission type organic EL display device, a switching element such as a thin film transistor which controls the drive voltage applied to the organic EL element, shuts out the light generated in the luminous layer of the organic EL layer (has an influence on the organic EL layer). Hence the aperture ratio for the generated light with respect the entire bottom surface of the device is reduced.

[0010] Therefore, recently, so that the switching element does not cause a shadow, development is progressing for a

top emission type organic EL display device where the upper section common electrode is made as a transparent or semi-transparent optical transmission electrode, and light is emitted from the upper electrode side.

[0011] In this case, for example the ITO constituting the common electrode of the upper section is formed at a low film forming temperature of 100° C. or less so as to not deteriorate the organic EL layer of the lower layer. Moreover in order to maintain the optical transmission, the film thickness is made approximately 150 nm.

[0012] However, generally for transparent conductive bodies, the electrical resistance is large to become 30 Ω per $\square$ with the aforementioned construction. In the organic EL element for the current drive, a large current is necessary at the time of high intensity emission, and due to the wiring resistance and the large current of the electrical path, an excessive load is applied to a power source.

[0013] That is to say, a voltage for where a voltage drop part comprising the product of the wiring resistance and the electrical current is subtracted from a power source voltage, becomes an effective voltage for the organic EL device.

[0014] In this case, since a resistivity of a metal wiring inside the TFT substrate is 0.2 ohms per $\square$, then for the wiring resistance and the voltage drop in the electrical path, the high resistance of the common electrode becomes a predominant factor. Since the common electrode is connected to the metal wiring inside the substrate at the outer periphery of the screen, then at the closest portion (screen outer periphery) and the remotest portion (the screen center) from the connecting locus of the common electrode, the length of the electrical path of the common electrode becomes different, so that the screen center has a high resistance load caused by the common electrode.

[0015] Moreover, when the whole screen is lit, that is to say, when all the pixels are energized, the current of each pixel becomes superimposed from the screen center towards the common electrode connection portion of the screen outer periphery. Therefore, the high resistance of the common electrode becomes multiplied so that the voltage drop of the screen center becomes greater than that for the screen outer periphery, and a difference occurs in the effective voltage of each of the organic EL elements, giving rise to brightness unevenness.

[0016] This brightness unevenness becomes a display quality loss. The larger the display is, the more conspicuous the brightness unevenness is since the area for light emission is large so that a large current is necessary and the common electrical path becomes long.

[0017] In order to solve the brightness unevenness which is apt to happen in the top emission type organic EL display device, as shown in Japanese Patent Application Laid-Open Nos. 2002-318556 and 2004-207217, a method is proposed where auxiliary wiring for the common electrode is arranged at a TFT substrate. This is explained with reference to **FIG. 16**.

[0018] **FIG. 16** is a schematic cross-section of a related art top emission type organic EL display device. A polysilicon island shape region 94 is formed on a glass substrate 91 via an SiN film 92 and an SiO₂ film 93. A gate electrode 96 made from Al is provided on the polysilicon island shape region 94

via a gate insulating film **95** made from SiO₂ film. An SiO₂ film **97** is provided so as to cover the whole surface, after which openings for the source-drain region are formed, and a source electrode **98** and a drain electrode **99** are formed, to thereby form a TFT as an active element.

[0019] Next, a positive type photosensitive polyimide is coated by a spin coating method, after which only the region corresponding to the source electrode **98** is exposed and developed, followed by baking. As a result, a flat insulating film **100** having contact holes **101** corresponding to the source electrode **98** is formed.

[0020] An Al film is deposited over the whole surface, after which a lower electrode **102** and auxiliary wiring **103** are formed by patterning in a predetermined shape. An SiO₂ film **104** is deposited over the whole surface, after which a through hole **105** which exposes the auxiliary wiring **103**, and an aperture area which exposes the lower electrode **102** are formed.

[0021] Using a vapor deposition mask which is positioned so that a non-aperture area corresponds to the auxiliary wiring **103**, a hole injection layer, a hole transport layer, and a light emitting layer are vapor deposited under heat in sequence to thereby form an organic EL layer **106**. The vapor deposition mask is then removed, and an upper electrode **107** made from ITO is deposited over the whole surface, and the upper electrode **107** and the auxiliary wiring **103** are electrically connected.

[0022] Finally, as with a normal organic EL device, sealing is performed in a dry nitrogen atmosphere, by means of a sealing plate **108** made from glass using a UV adhesive, to thereby complete the top emission type organic EL display device.

[0023] In this manner, the upper electrode **107** made from ITO of a high specific resistance, is connected to the auxiliary wiring **103** made from Al of a low specific resistance. As a result, the voltage drop due to the upper electrode **107** is reduced, and hence the display characteristics are greatly improved.

[0024] However, the whole screen comprises the pixel aperture area where the organic EL layer emits light, and the non pixel aperture area other than this, and if the space for the auxiliary wiring **103** and the through hole **105** which are constructed in the non pixel aperture area is to be kept large, the pixel aperture area becomes small and an aperture ratio (a ratio of the pixel aperture area with respect to the entire top surface of the device, same hereunder) is lowered so that the brightness is reduced. In the configuration of Japanese Patent Application Laid-Open No. 2004-207217, the aperture ratio is around 30%.

[0025] Furthermore, even if the non pixel aperture are made to the minimum value of the processing limits, the higher the definition of the device, the greater an occupation proportion of the non pixel aperture area, so that the aperture ratio is decreased. Therefore the configuration in the related arts is less advantageous for obtaining high intensity of light emission.

SUMMARY OF THE INVENTION

[0026] The present invention suppresses the area of a non pixel aperture area with the connection configuration for the

auxiliary wiring and the common electrode through the through holes, and therefore increases the aperture ratio.

[0027] A first aspect of the present invention is an organic EL display device which comprises a wiring layer, an insulating layer, first electrodes, an organic EL layer, and second electrodes, each laminated in sequence on a substrate, and all of the second electrodes are in a same layer. The organic EL display device further comprises a plurality of light emitting pixels which radiate light emitted from the organic EL layer and transmitted through the second electrode. Furthermore, wiring which conducts with the second electrode is arranged between the light emitting pixels, and is provided either between the organic EL layer and the second electrodes, or on top of the second electrodes, to give an organic EL display device.

[0028] By arranging the wiring which conducts with the second electrode between the light emitting pixels, the through holes become unnecessary, and the voltage drop due to the second electrodes can be reduced without changing the aperture ratio of the light emitting pixels.

[0029] In the above aspect, the plurality of the wiring, which conduct with the second electrode, may be configured so that film forming pattern of the respective wiring is continuous such that at least a portion of mutual patterns is overlapped. That is to say, a pattern of a vapor deposition mask which is used for respective wiring is superimposed- and wiring of a predetermined shape is optionally formed. As a result, it is not necessary to provide the aperture area at a high density on the vapor deposition mask which is used, and hence the rigidity of the vapor deposition mask can be increased.

[0030] Furthermore, the configuration may be such that the wiring which conducts with the second electrode has a so-called bus wiring in which alternate wirings intersect each other and being tied in a region outside of the light emitting pixels. As a result, the voltage drop can be reduced in the panel peripheral portion, where the current for each pixel passes through the wiring to be concentrated, and the current becomes large.

[0031] In the aforementioned aspect, the wiring may be configured to have a plurality of shape elements, and at least one part of the shape elements is mutually overlapped.

[0032] In the aforementioned aspect, the plurality of shape elements of the wiring may be arranged in mutually staggered form.

[0033] In the aforementioned aspect, the wiring may be configured such that the plurality of shape elements of the wiring which conduct with the second electrode include a plurality of types of shape elements, and at least a part of the shape elements of this plurality of types is mutually overlapped.

[0034] Also in each of the aforementioned aspects, the voltage drop due to the second electrode can be reduced without having an influence on the aperture ratio. Furthermore, by superimposing the pattern of the vapor deposition mask which is used, and optionally forming wiring of a predetermined shape, it is no longer necessary to provide aperture areas in a high density on the vapor deposition mask which is used, and the rigidity of the vapor deposition mask can be increased.

[0035] In the aforementioned aspect, the shape elements of the plurality of types of wiring which conducts with the second electrode comprise a first shape element and a second shape element, and the second shape element is arranged on an outer periphery of a region where the first shape element is arranged.

[0036] In the aforementioned aspect, the plurality of second shape elements may be arranged with positions shifted from each other, on an outer periphery of a region where the first shape element of the wiring which conducts with the second electrode is arranged.

[0037] According to each of the above aspects, the voltage drop due to the second electrode can be reduced without influencing the aperture ratio. Furthermore, the current of each pixel passes through the wiring and the current is concentrated, and the voltage drop in the panel peripheral portion where the current becomes large, can be reduced.

[0038] In a second aspect of the present invention, there is a vapor deposition mask which is used when constructing the organic EL display device, and which has a plurality of first aperture areas with a length L_1 and a width W_1 . The plurality of first aperture areas are arranged at a pitch P_1 in the length direction of the vapor deposition mask, and at a pitch P_2 in the width direction, and satisfy the relationships of $L_1 > P_1/2$, and $W_1 < P_2/2$.

[0039] As a result, it is not necessary to provide a high density aperture area on the vapor deposition mask, and the rigidity of the vapor deposition mask can be increased. Moreover, the dimensional accuracy of the aperture pattern of the vapor deposition mask can be easily maintained.

[0040] In the aforementioned aspect, second aperture areas of length L_2 and width W_2 may be multiply arranged in the width direction of the vapor deposition, so as to satisfy the relationships of pitch $P_3 = P_2 \times m$ (where m is an integer of one or more), and $W_2 < P_3$.

[0041] In the above aspect, third aperture areas of length L_3 and width W_2 may be multiply arranged in the width direction of the vapor deposition mask, so as to satisfy the relationships of pitch $P_3 = P_2 \times m$ (where m is an integer of one or more), and $W_2 < P_3$.

[0042] According to these aspects, a desired wiring is obtained without providing a high density aperture area for the vapor deposition mask. Consequently, the rigidity of the vapor deposition mask can be increased, and the dimensional accuracy of the aperture pattern of the vapor deposition mask is easily maintained.

[0043] In the aforementioned aspect, third aperture areas arranged at a pitch P_3 may be arranged in the mutual length direction, with the position shifted by δ satisfying $\delta < L_3$.

[0044] By using such a vapor deposition mask, bus wiring can be laid and deposited in optional directions.

[0045] In the aforementioned aspect, a slit aperture of width W_1 may be provided in the vicinity of the width W_2 of the third aperture area of the vapor deposition mask.

[0046] In the aforementioned aspect, a slit aperture area in the vicinity of the width W_2 of the third aperture area of the vapor deposition mask, may be arranged at two or more locations, and the slit aperture area may be arranged so that a pitch $P_4 = P_2 \times k$ (where k is an integer of one or more) in the

width direction of the first aperture area is satisfied, and the first aperture area is provided between a plurality of the slit aperture areas arranged in parallel.

[0047] By using such a vapor deposition mask, wiring wherein the third aperture area and the first aperture area are superimposed is obtained by means of the slit aperture.

[0048] Furthermore, since a highly detailed wiring pattern configuration is obtained without forming a high density aperture area in the vapor deposition mask, the rigidity of the vapor deposition mask can be increased.

[0049] In the aforementioned aspect, the plurality of second aperture areas may be provided on the outer periphery of a region where the plurality of first aperture areas is arranged.

[0050] In the aforementioned aspect, the plurality of third aperture areas may be provided on the outer periphery of a region where the plurality of first aperture areas is arranged.

[0051] By using such a vapor deposition mask, the current of each pixel passes through the wiring and the current is concentrated, and a wiring is obtained which can reduce the voltage drop in the panel peripheral portion where the current becomes large.

[0052] A third aspect of the present invention is a manufacturing method for an organic EL display device. The organic EL display device comprises laminating on a substrate in sequence from the substrate side, a wiring layer, an insulating layer, a first electrode, an organic EL layer, and a second electrode and forming all of the second electrodes in the same layer. The display device has a plurality of light emitting pixels which radiate light emitted from the organic EL layer and is transmitted through the second electrode. The manufacturing method comprises either before or after forming the second electrodes, the aforementioned vapor deposition mask is used to deposit wiring material on the substrate, and then the aforementioned vapor deposition mask is moved with respect to the substrate on which the wiring material has been deposited by $(P_2/2) \times (2n-1)$ (where n is an integer of one or more) in the width direction of the first aperture area of the vapor deposition mask, and further the wiring material is deposited, to thereby form a wiring which conducts with the second electrode.

[0053] By the aforementioned manufacturing method, a desired wiring can be obtained without providing a high density aperture area on the vapor deposition mask, and the voltage drop due to the second wiring layer can be reduced without having an influence on the aperture ratio. Furthermore, the rigidity of the vapor deposition mask is improved, and dimensional accuracy of the aperture pattern is easily maintained.

[0054] In the embodiments of the invention, by directly forming the auxiliary wiring on the upper face or lower face of the common electrode, the connection between the common electrode and the auxiliary wiring is reliably obtained, and a through hole connection configuration becomes unnecessary. Therefore the aperture ratio can be increased, the voltage drop due to the second electrode can be reduced, and a high intensity can be obtained.

[0055] In particular, by making the aperture pattern in the vapor deposition mask for forming the auxiliary wiring, a mesh pattern by the aperture dimensions and the arrange-

ment pitch, a desired wiring is obtained, and also the rigidity of the vapor deposition mask is improved, and the dimensional accuracy of the aperture pattern is easily maintained.

BRIEF DESCRIPTION OF THE DRAWINGS

[0056] Embodiments of the present invention will be described in detail based on the following figures, wherein:

[0057] **FIG. 1** is an explanatory drawing of a fundamental configuration of one embodiment of the present invention;

[0058] **FIG. 2** is a schematic cross-section view of a top emission type organic EL device of a first example of the present invention;

[0059] **FIG. 3** is an explanatory drawing of formation for inter-pixel auxiliary wiring;

[0060] **FIG. 4** is an explanatory drawing of formation for an auxiliary wiring connection portion;

[0061] **FIG. 5A** and **FIG. 5B** are explanatory drawings of a resistance drop effect of a common electrode due to the auxiliary wiring;

[0062] **FIG. 6** is a schematic cross-section view of a top emission type organic EL device of a second example of the present invention;

[0063] **FIG. 7** is a plan view showing an overall vapor deposition mask used in a third example of the present invention;

[0064] **FIG. 8** is an enlarged view of a pattern region corner of the vapor deposition mask;

[0065] **FIG. 9** is an explanatory drawing of a slit aperture area;

[0066] **FIG. 10** is an explanatory drawing of formation for auxiliary wiring of the third example;

[0067] **FIG. 11** is an enlarged view of a pattern region corner of a vapor deposition mask used in the fourth example of the present invention;

[0068] **FIG. 12** is an explanatory drawing of a slit aperture area;

[0069] **FIG. 13** is an explanatory drawing of formation for auxiliary wiring of the fourth example;

[0070] **FIG. 14** is an explanatory drawing of formation for auxiliary wiring of a fifth example;

[0071] **FIG. 15** is an explanatory drawing of formation for auxiliary wiring of a sixth example; and

[0072] **FIG. 16** is a schematic cross-section view of a related art top emission type organic EL display device.

DETAILED DESCRIPTION OF THE INVENTION

[0073] In one embodiment of the present invention, a wiring layer, an insulating layer, a first electrode, and an organic EL layer are sequentially laminated on a substrate. Either before or after forming a second electrode, wiring material is vapor deposited on the substrate via a vapor deposition mask on which a plurality of first apertures of length L_1 and width W_1 are arranged at a pitch P_1 in the length direction thereof, and at a pitch P_2 in the width

direction, so as to satisfy a relationship of $L_1 > P_1/2$, and $W_1 < P_2/2$. Furthermore, the wiring material is vapor deposited with the vapor deposition mask moved with respect to the substrate by just $(P_2/2) \times (2n-1)$ (where n is an integer of one or more) in the width direction of the first aperture area, and auxiliary wiring which conducts with a second electrode is formed.

First Example

[0074] Here, a top emission type organic EL display device of a first example of the present invention is explained, with reference to **FIG. 2** through **FIG. 5**.

[0075] As shown in **FIG. 2**, at first, pixel circuits **12** for controlling the electric light emission of each pixel are formed on an insulation substrate **11** made of a glass, resin film, or the like after which pixel electrodes **14** corresponding to each pixel circuit **12** are formed via an interlaminar insulating layer **13**.

[0076] These pixel electrodes **14** are electrically connected to the pixel circuits **12** via contact holes (not shown) provided in the interlaminar insulating layer **13**.

[0077] Next, an organic EL layer **15** and a common electrode **16** made from ITO, are sequentially mask vapor deposited on each of the pixel electrodes **14**, after which, in order to evenly reduce the resistance of the common electrode **16**, Al or Ag is vapor deposited using a vapor deposition mask, to thereby form auxiliary wiring **17** between the pixels (inter-pixel auxiliary wiring **18**) and on the screen outer periphery (auxiliary wiring connection portion **19**).

[0078] **FIG. 3** is an explanatory drawing of the formation for the inter-pixel auxiliary wiring **18**. Using a vapor deposition mask **21** having lengthwise stripe shape aperture areas **22** arranged at a spacing corresponding to the pixel pitch, inter-pixel auxiliary wiring **18** is formed on the common electrode **16** provided on the insulation substrate **11**.

[0079] **FIG. 4** is an explanatory drawing of the formation for the auxiliary wiring connection portion **19**. Using a vapor deposition mask **23** having two transverse stripe shape aperture areas **24**, auxiliary wiring connection portions **19** are formed outside of the pixel region of the common electrode **16** which is provided with the inter-pixel auxiliary wiring **18**. The each auxiliary wiring connection portion **19** has wider width than the each inter-pixel auxiliary wiring **18**.

[0080] In particular, in forming a multi-colored organic EL layer such as an RGB three primary color layer for obtaining a full color display, since a space is provided between the light emitting pixels (between pixel electrodes) for separately coating the colors, the auxiliary wiring **17** is provided on this space so that it does not projectively overlap with the pixel electrodes **14**.

[0081] In the first example of the present invention, since the inter-pixel auxiliary wiring **18** is provided between the pixels, the resistance of the common electrode **16** made from ITO can be evenly reduced without changing the aperture area (the aperture ratio) of the organic EL layer, and hence brightness unevenness can be effectively reduced.

[0082] Furthermore, since the auxiliary wiring connection portions **19** which have wider width than the inter-pixel auxiliary wiring **18**, are provided outside the pixel region

where the most current flows, the voltage drop due to the large electric current outside of the pixel region can be reduced.

[0083] FIG. 5A and FIG. 5B are explanatory drawings of a resistance drop effect of the common electrode due to the auxiliary wiring. FIG. 5A is an explanatory drawing of a measurement method, and FIG. 5B is an explanatory drawing of measurement results.

[0084] As shown in FIG. 5A, external connection terminals for the common electrode are provided at four corners of the panel. The resistances of the common electrode according to the distance up to the screen center are measured, with the respective outside connection terminals as the starting point.

[0085] For the common terminal in this case, ITO of a thickness of 300 nm is used, and a panel provided with auxiliary wiring made from Ag of a thickness of 200 nm is measured. For comparison, a comparative example 1 provided with a common electrode of ITO with a thickness of 300 nm, and a comparative example 2 of a bottom emission type which uses Al of a thickness of 200 nm for the common electrode, are shown together.

[0086] As shown in FIG. 5B, in the comparative example 1, at a resistance distribution at 18 to 24 ohms, an intensity unevenness is seen where the low resistance screen corners emit in high intensity, while the high resistance screen center emits in low intensity.

[0087] On the other hand, in the case of the example 1 of the present invention, the resistance distribution becomes 3 to 4 ohms, which is a little higher than the 1 to 2 ohms of the comparative example 2, however, the intensity unevenness is hardly visible similar to the comparative example 2.

Second Example

[0088] A top emission type organic EL display device of a second example of the present invention is described with reference to FIG. 6. Since the vapor deposition mask which is used is the same as for the first example except that the position where the auxiliary wiring is provided is different, then only the cross-section configuration is shown.

[0089] As with the first example, pixel circuits 12 for controlling the electric light emission of each pixel are formed on an insulation substrate 11, after which pixel electrodes 14 corresponding to each pixel circuit 12 are formed via an interlaminar insulating layer 13. Then an organic EL layer 15 is vapor deposited on the pixel electrodes 14.

[0090] So that the organic EL layer is not deteriorated by moisture or oxygen and the like, the aforementioned vapor deposition mask 21 and a vapor deposition mask 23 are used, and inter-pixel auxiliary wiring 18 and auxiliary wiring connection portions 19 are vacuum formed in sequence manner on the organic EL layer 15. Then after forming auxiliary wiring 17, a common electrode 16 made from ITO is vapor deposited over the whole surface.

[0091] The resistance of the common electrode 16 can be evenly reduced, and the intensity unevenness can be effectively reduced without changing the aperture ratio of the organic EL layer. Furthermore, the voltage drop due to the large current outside of the pixel region can be reduced.

[0092] However, in the aforementioned first and second examples, forming the vapor deposition mask 21 having the aforementioned lengthwise stripe shape aperture areas 22 is difficult, and in particular, as stripe shape aperture areas 22 become highly detailed (narrow pitch), slippage deformation of the pattern accompanying a rigidity deterioration of the stripe portion occurs, and hence it becomes difficult to maintain the stripe shape.

[0093] In order to keep the stripe shape, the mask rigidity can be maintained by thinning a number of the stripes, however it becomes necessary to add a vapor deposition process for the thinned portion.

Third Example

[0094] A third example of the present invention is described. However since the basic structure is the same as for the aforementioned first example and second example, only the vapor deposition mask and the vapor deposition pattern are described.

[0095] FIG. 7 is a plan view showing the overall vapor deposition mask used in the third example of the present invention. Furthermore, FIG. 8 is an enlarged view of a pattern region corner of the vapor deposition mask. The vapor deposition mask 31 comprises slit aperture areas 32 for inter-pixel auxiliary wiring, and slit aperture areas 33 and slit aperture areas 34 constituting auxiliary wiring connection portions.

[0096] FIG. 9 is an explanatory drawing of the slit aperture areas of the deposition mask 31. The slit aperture area 32 for the inter-pixel auxiliary wiring is length L_1 and width W_1 , and the slit aperture area 33 is length L_2 and width W_2 . The slit aperture area 34 comprises a slit portion 35 of length $L_1/2$ and width W_1 , a rectangular portion 36 of length L_3 and width W_2 , and a connection portion 37.

[0097] As shown in FIG. 8, the slit aperture areas 32 for the inter-pixel auxiliary wiring are arranged at a pitch P_1 in the length direction, and a pitch P_2 in the width direction, thereof. Another slit aperture areas 32 are further arranged in positions of half of the respective pitches P_1 and P_2 , giving a staggered array.

[0098] Furthermore, the slit aperture areas 33 and the slit aperture areas 34 are arranged at a pitch P_3 in the width direction thereof.

[0099] The slit portion 35 provided in the slit aperture area 34 must be positioned corresponding to the edge of the staggered array of the slit aperture areas 32, and hence P_2 is determined to be same to P_3 .

[0100] Furthermore, some of slit aperture areas 34 are configured shifted by δ in the length direction, so that a bus wiring in an optional inclined direction can be formed.

[0101] FIG. 10 is an explanatory drawing of formation for the auxiliary wiring of the third example. The aforementioned vapor deposition mask 31 is arranged at an origin position and film forming is performed to thereby form inter-pixel auxiliary wiring elements 42 and auxiliary wiring connection elements 45 and 47 (bus wiring element 45 and 47).

[0102] At this time, the origin position is set so that the slit aperture areas 32 are positioned in the regions between the adjacent pixel electrodes 14.

[0103] A film is formed at a position where the vapor deposition mask is moved by $P_3/2=P_2/2$ in the width direction of the respective slit aperture areas, so that an inter-pixel auxiliary wiring elements **43**, and bus wiring elements **46** and **48** are formed with being partly overlapped with the inter-pixel auxiliary wiring elements **42** and the bus wiring elements **45** and **47**, respectively, which are previously formed. A plurality of inter-pixel auxiliary wiring **41** and bus wiring **44** are thereby formed.

[0104] A patterning overlapped width D of the respective slit aperture areas is determined as follows from the relationship of the pattern dimensions of the aforementioned slit aperture areas.

[0105] An overlap D_1 in the length direction of the inter-pixel auxiliary wiring elements **42** and **43** becomes:

$$D_1=L_1-P/2$$

[0106] Furthermore, an overlap D_2 in the length direction of the inter-pixel auxiliary wiring elements **42** or **43**, and the bus wiring elements **45** or **46** becomes:

$$D_2=L_1-P/2$$

[0107] Moreover, an overlap D_3 in the width direction in each of the bus wiring elements **45** and **46**, the bus wiring elements **47** and **48**, or the bus wiring elements **46** and **47** becomes:

$$D_3=W_2-(P_3/2)$$

[0108] One example of the numerical values for the case where the auxiliary wiring is formed with the aforementioned vapor deposition mask **31**, for a display device of RGB tricolor configuration is shown in Table 1.

TABLE 1

Image size	64 mm × 48 mm	3.2 type
Pixel number	320 × 240	QVGA specification
Pixel pitch	0.2 mm	Definition 127 ppi
Sub-pixel region	0.067 mm × 0.2 mm	RGB tricolor configuration
Pixel electrode	0.042 mm × 0.19 mm	Aperture ratio 60%
Auxiliary wiring mask	P1	0.5 mm
	P2	0.134 mm
	P3	0.134 mm
	L1	0.27 mm
	W1	0.02 mm
	L2	2.5 mm
	W2	0.1 mm
Auxiliary wiring	D1	0.02 mm
film overlapped	D2	0.02 mm
width	D3	0.033 mm

[0109] In the third example of the present invention, since the stripe shape aperture area in which each stripe shape aperture has continuous long shape is not provided, the rigidity of the vapor deposition mask is increased, and the slippage deformation of the pattern can be suppressed. Furthermore, since the vapor depositions are performed two times, being the same as for the first example or the second example, the manufacturing processes are not increased.

Fourth Example

[0110] A fourth example of the present invention is described with reference to FIG. 11 through FIG. 13.

However since the basic device structure is the same as for the aforementioned first example or second example, only the vapor deposition mask and the vapor deposition pattern is described.

[0111] FIG. 11 is an enlarged view of a pattern region corner of a vapor deposition mask used in the fourth example of the present invention. The vapor deposition mask **51** comprises slit aperture areas **52** for inter-pixel auxiliary wiring, and slit aperture areas **54** and slit aperture areas **53** constituting auxiliary wiring connection portions.

[0112] FIG. 12 is an explanatory drawing of the slit aperture areas. The slit aperture area **52** for the inter-pixel auxiliary wiring is length L_1 and width W_1 , and the slit aperture area **53** for the auxiliary wiring connection portion is length L_2 and width W_2 . Moreover, for the slit aperture area **54**, on a tip end portion of a rectangular portion **56** of length L_3 and width W_2 there is provided three slit portions **55** at a pitch of P_4 , of a length $L_1/2$ and width W_1 .

[0113] As shown in FIG. 11, the slit aperture areas **52** for the inter-pixel auxiliary wiring are arranged at a pitch P_1 in the length direction thereof, and a pitch P_2 in the width direction thereof. Moreover another slit aperture areas **52** are arranged in positions of half of the respective pitches P_1 and P_2 , giving a staggered array.

[0114] Furthermore, the slit aperture areas **53** and the slit aperture areas **54** are arranged at a pitch P_3 in the width direction thereof.

[0115] The slit portions **55** provided in the slit aperture area **54** must be positioned at the edge of the staggered array of the slit aperture areas **52**, and hence the pitches are determined as $P_2 \times 3 = P_3$.

[0116] Furthermore, the plurality of slit aperture areas **54** is configured shifted by 6 in the length direction, so that a bus wiring in an optional inclined direction can be formed.

[0117] FIG. 13 is an explanatory drawing of formation for the auxiliary wiring of the fourth example. Film forming is performed using the aforementioned vapor deposition mask **51** at an origin position, to thereby form inter-pixel auxiliary wiring elements **62** and auxiliary wiring connection elements **65** and **67** (bus wiring elements **65** and **67**).

[0118] At this time, the origin position is set so that the slit aperture areas **52** are positioned in the regions between the adjacent pixel electrodes **14**.

[0119] Next, a film is formed at a position where the vapor deposition mask is moved by $P_3/2=P_2 \times 3/2$ in the width direction of the respective slit aperture areas, so that an inter-pixel auxiliary wiring elements **63**, and bus wiring elements **66** and **68** are partly overlapped, respectively with the inter-pixel auxiliary wiring elements **62** and the bus wiring elements **65** and **67** which are formed previously. Thereby, inter-pixel auxiliary wiring **61** and bus wiring **64** are formed.

[0120] Respective patterning overlapped widths D are determined as follows from the relationship of the aforementioned pattern dimensions.

[0121] An overlap D_1 in the length direction of the inter-pixel auxiliary wiring elements **62** and **63** becomes:

$$D_1=L_1-P_1/2$$

[0122] Furthermore, respective overlaps D_2 in the length direction of the inter-pixel auxiliary wiring elements **62** and **63**, and the bus wiring elements **65** and **66** becomes:

$$D_2 = L_1 - P_1/2$$

[0123] Moreover, an overlap D_3 in the width direction in each of the bus wiring elements **65** and **66**, the bus wiring elements **67** and **68**, or the bus wiring elements **66** and **67** becomes:

$$D_3 = W_2 - (P_3/2)$$

[0124] One example of the numerical values for a case where an auxiliary wiring is formed with the aforementioned vapor deposition mask **51**, for a display device of a RGB tricolor configuration is shown in Table 2.

TABLE 2

Image size	64 mm × 48 mm	3.2 type
Pixel number	320 × 240	QVGA specification
Pixel pitch	0.2 mm	Definition 127 ppi
Sub-pixel region	0.067 mm × 0.2 mm	RGB tricolor configuration
Pixel electrode	0.042 mm × 0.19 mm	Aperture ratio 60%
Auxiliary wiring mask	P1 0.5 mm	Optional
	P2 0.134 mm	Two times sub-pixel pitch
	P3 0.402 mm	$P3 = P2 \times 3$
	L1 0.27 mm	$L1 > (P1/2)$
	W1 0.02 mm	Less than 0.025 mm between pixel electrodes
	L2 2.5 mm	Optional
	W2 0.25 mm	$W2 > (P3/2)$
Auxiliary wiring	D1 0.02 mm	$D1 = L1 - (P1/2)$
film overlap	D2 0.02 mm	$D2 = L1 - (P1/2)$
width	D3 0.049 mm	$D3 = W2 - (P3/2)$

[0125] In the fourth example of the present invention, since the stripe shape aperture area in which each stripe shape aperture has continuous long shape is not provided, the rigidity of the vapor deposition mask is increased, and the slippage deformation of the pattern can be suppressed. Furthermore, since the vapor depositions are performed two times, being the same as for the first example or the second example, the manufacturing processes are not increased.

[0126] Moreover, in the fourth example, the slit aperture areas **53** and **54** are formed to be wide in width direction thereof Therefore, in the case of high definition, the space between the slit aperture areas **53**, **54** pairs, that is, the support portion for the vapor deposition mask, can be made wide. Hence the rigidity of the mask can be further increased.

Fifth Example

[0127] A fifth example of the present invention is described with reference to **FIG. 14**. Since the basic device structure is the same as for the aforementioned fourth example, only the formation for the auxiliary wiring are described.

[0128] A transverse direction slit is provided in the central portion of the slit aperture area **52** in the aforementioned vapor deposition mask **51**, and film forming is performed at an origin position using a vapor deposition mask made with cross-shape aperture areas, to thereby form inter-pixel auxiliary wiring elements **72** and bus wiring elements **75** and **77**.

[0129] At this time, the origin position is set so that the cross-shape aperture areas are positioned in the regions between the adjacent pixel electrodes **14**.

[0130] Next, a film is formed at a position where the vapor deposition mask is moved by $P_3/2 = P_2 \times 3/2$ in the width direction of the respective slit aperture areas, so that inter-pixel auxiliary wiring element **73**, and bus wiring element **76** and **78** are partly overlapped, respectively with the inter-pixel auxiliary wiring elements **72** and the bus wiring elements **75** and **77** which are formed previously. Thereby, inter-pixel auxiliary wiring **71** and bus wiring **74** are formed.

[0131] In this fifth example, since the cross-shape aperture areas are provided, a mesh shape inter-pixel auxiliary wiring can be formed, and the transmission resistance of the common electrode can be further reduced. Moreover, even if tearing of the auxiliary wiring due to mask defects occurs in one direction of the cross-shape wiring, a current is supplied from the other direction wiring, and hence there is no loss of uniformity of the resistance of the common electrode.

Sixth Example

[0132] A sixth example of the present invention is described with reference to **FIG. 15**. Since the basic device structure is the same as for the aforementioned fourth example, only the formation for the auxiliary wiring is described.

[0133] In the vapor deposition mask of this example, compared to the single slit aperture **52** in the aforementioned vapor deposition mask **51**, a transverse direction slit is provided for connecting between adjacent single slit apertures **52** which are provided at staggered positions, to give a crank-shape aperture area. Film forming is performed at an origin position using this vapor deposition mask, to thereby form inter-pixel auxiliary wiring elements **82** and bus wiring elements **85** and **87**.

[0134] At this time, the origin position is set so that the crank-shape aperture areas are positioned in the regions between the adjacent pixel electrodes **14**.

[0135] Next, a film is formed at a position where the vapor deposition mask is moved by $P_3/2 = P_2 \times 3/2$ in the width direction of the respective slit aperture areas, so that inter-pixel auxiliary wiring elements **83**, and bus wiring elements **86** and **88** are overlapped, respectively with the inter-pixel auxiliary wiring elements **82**, and the bus wiring elements **85** and **87** which are formed previously. Thereby, inter-pixel auxiliary wiring **81** and bus wiring **84** are formed.

[0136] In the sixth example, since the crank-shape aperture areas are provided, then as for the aforementioned fifth example, a mesh shape inter-pixel auxiliary wiring can be formed, and the transmission resistance of the common electrode can be further reduced. Moreover, even if tearing of the auxiliary wiring due to mask defects occurs in one direction of the crank-shape wiring, a current is supplied from the other direction wiring, and hence there is no loss of uniformity of the resistance of the common electrode.

[0137] In the above, various examples of the present invention have been described, however the present invention is not limited or construed to the conditions and configurations described for the respective examples, and various modifications are possible. For example, in the

aforementioned respective examples, the configuration of the organic EL layer is not shown, however this is appropriately selected from amongst known organic EL materials in accordance with the luminescent colors.

[0138] Furthermore, in the aforementioned respective examples, ITO is used as the translucent material constituting the common electrode. However this is not limited to ITO, and other transparent oxide conductive materials such as IZO or ZnO may be used. Moreover, a metallic thin film of for example Al or Ag formed as a thin film of approximately 20 nm may be used.

[0139] Furthermore also in the case of the aforementioned third example, the slit aperture area used for the inter-pixel auxiliary wiring may be a cross-shape aperture area or a crank-shape aperture area as in the fifth example or the sixth example, thereby a mesh shape inter-pixel auxiliary wiring can be formed.

[0140] Moreover, in the aforementioned respective examples, a glass substrate is used as the substrate. However since the display devices of the respective embodiments are a top emission type, the substrate need not be transparent, and a conducting substrate such as of stainless steel, or a nonconductive opaque substrate may be used.

[0141] Furthermore, in the aforementioned respective examples, the description has been for a full color display device. However the invention is applicable to a different hue glass display device where a plurality of colors are appropriately combined. Moreover, the invention is also applicable to the case of constructing a single color display device.

[0142] As an applicable example of the present invention, a two dimensional matrix display device is a typical example, but the present invention is not limited to the display device, and can be applied to a large-size single light source such as a light source for mood illumination.

What is claimed is:

1. An organic electroluminescent display device comprising a wiring layer, an insulating layer, a first electrode, an organic electroluminescent layer, and a second electrode that are laminated on a substrate in sequence from the substrate side, wherein:

all of the second electrodes are in the same layer;

the organic electroluminescent display device has a plurality of light emitting pixels radiating light that is emitted from the organic electroluminescent layer and is transmitted through the second electrode; and

the organic electroluminescent display device further comprises wiring that conducts with the second electrode, the wiring being arranged between the light emitting pixels and being provided either between the organic electroluminescent layer and the second electrodes or on top of the second electrodes.

2. The organic electroluminescent display device according to claim 1, wherein the wiring is configured to be continuous such that at least a part of mutual film forming patterns of the respective wiring is overlapped.

3. The organic electroluminescent display device according to claim 2, wherein alternate wirings intersect so as to be connected to each other in a region corresponding to a region outside of the light emitting pixels.

4. An organic electroluminescent display device comprising:

a substrate;

a wiring layer;

an insulating layer;

a first electrode;

an organic electroluminescent layer;

a second electrode; and

wiring which conducts with the second electrode, wherein all of the second electrodes are in the same layer,

the organic electroluminescent display device has a plurality of light emitting pixels radiating light that is emitted from the organic electroluminescent layer and is transmitted through the second electrode, and

the wiring is arranged between the light emitting pixels, and is provided either between the organic electroluminescent layer and the second electrodes, or on top of the second electrodes.

5. The organic electroluminescent display device according to claim 4, wherein the wiring comprises a plurality of shape elements and at least a part of the shape elements is mutually overlapped.

6. The organic electroluminescent display device according to claim 5, wherein the plurality of shape elements are arranged in a mutually staggered form.

7. The organic electroluminescent display device according to claim 5, wherein the plurality of shape elements includes a plurality of types of shape elements, and constitutes the wiring in which at least a part of the shape elements of the plurality of types is mutually overlapped.

8. The organic electroluminescent display device according to claim 7, wherein the shape elements of the plurality of types comprise a first shape element and a second shape element, and the second shape element is arranged on an outside periphery of a region where the first shape element is arranged.

9. The organic electroluminescent display device according to claim 8, wherein the plurality of second shape elements are arranged with positions thereof shifted from each other on the outside periphery of the region where the first shape element is arranged.

10. A vapor deposition mask which has a plurality of first aperture areas with a length L_1 and a width W_1 , respectively, wherein the plurality of first aperture areas are arranged at a pitch P_1 in the length direction of the vapor deposition mask, and at a pitch P_2 in the width direction of the vapor deposition mask, and satisfy the relationships of $L_1 > P_1/2$, and $W_1 < P_2/2$.

11. The vapor deposition mask according to claim 10, wherein second aperture areas of length L_2 and width W_2 , respectively, are multiply arranged in the width direction of the vapor deposition mask, so as to satisfy the relationships of pitch $P_3 = P_2 \times m$ (where m is an integer of one or more), and $W_2 < P_3$.

12. The vapor deposition mask according to claim 11, wherein third aperture areas of length L_3 and width W_2 , respectively, are multiply arranged in the width direction of the vapor deposition mask, so as to satisfy the relationships of pitch $P_3 = P_2 \times m$ (where m is an integer of one or more), and $W_2 < P_3$.

13. The vapor deposition mask according to claim 12, wherein the third aperture areas are arranged with the position shifted by δ satisfying $\delta < L_3$ in the length direction thereof.

14. The vapor deposition mask according to claim 12, wherein a slit aperture of width W_1 is provided in the vicinity of the width W_2 of the third aperture area.

15. The vapor deposition mask according to claim 12, wherein a slit aperture in the vicinity of the width W_2 of the third aperture area, is arranged at two or more locations, and the slit aperture area is arranged at a pitch $P_4 = P_2 \times k$ (where k is an integer of one or more) in the width direction of the first aperture area, and the first aperture area is provided between a plurality of the slit aperture areas arranged in parallel.

16. The vapor deposition mask according to claim 11, wherein the plurality of second aperture areas are provided on an outside periphery of a region where the plurality of first aperture areas are arranged.

17. The vapor deposition mask according to claim 12, wherein the plurality of third aperture areas are provided on an outside periphery of a region where the plurality of first aperture areas are arranged.

18. A manufacturing method for an organic electroluminescent display device comprising a wiring layer, an insulating layer, a first electrode, an organic electroluminescent layer, and a second electrode that are laminated on a substrate, wherein all of the second electrodes are formed in the same layer, and the display device has a plurality of light emitting pixels radiating light that is emitted from the organic electroluminescent layer and is transmitted through the second electrode, said method comprising:

either before or after forming the second electrodes, depositing wiring material on the substrate using the vapor deposition mask according to claim 10, and

moving the vapor deposition mask according to claim 10 with respect to the substrate on which the wiring material has been deposited by $(P_2/2) \times (2n-1)$ (where n is an integer of one or more) in the width direction of the first aperture area of the vapor deposition mask, and further depositing the wiring material, to thereby form a wiring which conducts with the second electrode.

* * * * *

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摘要(译)

在包括布线层，绝缘层，第一电极，有机电致发光层和第二电极的有机电致发光显示装置中，与第二电极导电的布线布置在发光像素之间，并且设置在有机电致发光显示装置之间。电致发光层和第二电极，或在第二电极的顶部。

